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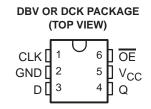
- **Qualified for Automotive Applications**
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Ioff Supports Partial-Power-Down Mode Operation

description/ordering information

This single D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G374 features a 3-state output designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



On the positive transition of the clock (CLK) input, the Q output is set to the logic level set up at the data (D) input.

A buffered output-enable ($\overline{\mathsf{OE}}$) input can be used to place the output in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION[†]

TA	PACKAGE [‡]	PACKAGE [‡]		TOP-SIDE MARKING§
1000 1- 10500	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G374QDBVRQ1	CA40
–40°C to 125°C	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G374QDCKRQ1	D40

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

§ DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



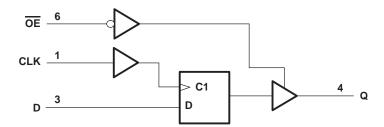
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FU	NC.	TIO	ΝТ	ABI	F

	1 011011	011 1/1	
	INPUTS	OUTPUT	
OE	CLK	D	Q
L	\uparrow	L	L
L	\uparrow	Н	н
L	H or L	Х	Q
Н	Х	Х	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, V_{C}	
(see Note 1)	
Voltage range applied to any output in the high or low state, V_{O}	
(see Notes 1 and 2)	$\dots -0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} (V _O < 0)	
Continuous output current, I _O	
Continuous current through V _{CC} or GND	
Package thermal impedance, θ _{JA} (see Note 3): DBV package	
DCK package	
Storage temperature range, T _{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. The value of V_{CC} is provided in the recommended operating conditions table.

3. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 4)

			MIN	MAX	UNI	
.,		Operating	1.65	5.5		
VCC	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
		V _{CC} = 2.3 V to 2.7 V	1.7			
VIH	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
.,		V _{CC} = 2.3 V to 2.7 V		0.7	.,	
VIL	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
VI	Input voltage	·	0	5.5	V	
Vo	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
				-16		
ЮН	High-level output current	$V_{CC} = 3 V$		-24	mA	
		V _{CC} = 4.5 V		-32		
		$V_{CC} = 5 \text{ V}, \text{ T}_{A} = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$		-40		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
				16		
IOL	Low-level output current	V _{CC} = 3 V		24	mA	
		V _{CC} = 4.5 V		32		
		$V_{CC} = 5 \text{ V}, \text{ T}_{A} = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$	40			
		V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/\	
		V_{CC} = 5 V ± 0.5 V		5		
ТА	Operating free-air temperature		-40	125	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			$T_A = -40$	°C TO 8	5°C	T _A = -40	°C TO 12	5°C		
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP†	MAX	MIN	түр†	MAX	UNI	
	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			1.2				
	I _{OH} = -8 mA	2.3 V	1.9			1.9				
VOH	I _{OH} = -16 mA		2.4			2.4			V	
011	I _{OH} = -24 mA	3 V	2.3			2.3				
	I _{OH} = -32 mA	4.5 V	3.8			3.8				
	I _{OH} = -40 mA	5 V	4.4							
	I _{OL} = 100 μA	1.65 V to 5.5 V			0.1			0.1		
	I _{OL} = 4 mA	1.65 V			0.45			0.45		
	I _{OL} = 8 mA	2.3 V			0.3			0.3	0.3	
VOL	I _{OL} = 16 mA				0.4			0.5	v	
· OL	I _{OL} = 24 mA	3 V			0.55			0.65	•	
	I _{OL} = 32 mA	4.5 V			0.55			0.65		
	I _{OL} = 40 mA	5 V			0.513					
l	$V_{I} = 5.5 V \text{ or GND}$	0 to 5.5 V			±1			<u>+2</u>	μA	
I _{OZ}	$V_{O} = 0$ to 5.5 V	1.65 V to 5.5 V			±5			±12	μA	
loff	$V_{I} \text{ or } V_{O} = 5.5 \text{ V}$	0			±10			±25	μA	
ICC	$V_{I} = 5.5 \text{ V or GND}, I_{O} = 0$	1.65 V to 5.5 V			10			10	μA	
ΔICC	One input at $V_{CC} - 0.6 V$, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	μA	
Ci	$V_I = V_{CC}$ or GND	3.3 V		3			3		pF	
Co	$V_{O} = V_{CC}$ or GND	3.3 V		6			6		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		100		125		150		175	MHz
tw	Pulse duration, CLK high or low	3.3		3		2.8		2.5		ns
t _{su}	Setup time, data before CLK [↑]	3.5		2.5		2		1.5		ns
th	Hold time, data after CLK↑	3.4		1.6		1.5		1.5		ns



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switching characteristics over free-air temperature range of -40° C to 85° C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			100		125		150		175		MHz
^t pd	CLK	Q	2.7	18.3	1.8	8.2	1.6	6	1	4	ns
t _{en}	OE	Q	2	13	1.5	6.3	0.9	5	0.7	3.5	ns
^t dis	OE	Q	2	14	1.1	5.3	1.4	4.5	0.8	3.1	ns

switching characteristics over free-air temperature range of -40° C to 125° C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			100		125		150		175		MHz
^t pd	CLK	Q	2.7	18.3	1.8	10.2	1.6	7	1	5	ns
t _{en}	OE	Q	2	14	1.5	8.3	0.9	6.5	0.7	5.5	ns
^t dis	OE	Q	2	16	1.1	7.3	1.4	6	0.8	5.1	ns

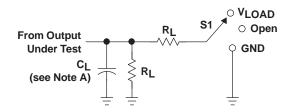
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT	
<u> </u>	Power dissipation	dissipation Outputs enabled		24	24	25	27		
Cpd	capacitance	Outputs disabled	f = 10 MHz	8	8	9	11	р⊦	



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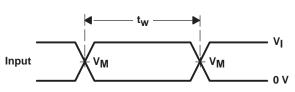
PARAMETER MEASUREMENT INFORMATION



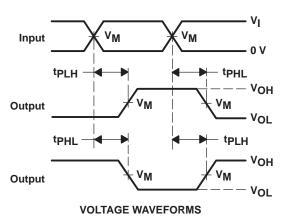
LOAD CIRCUIT

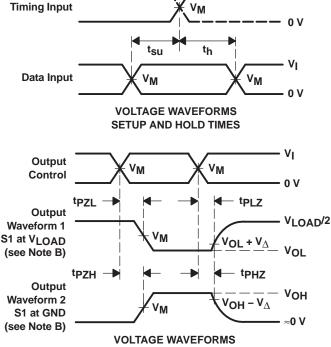
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
^t PHZ ^{/t} PZH	GND

	INF	PUTS	N	N N	•	-	N
Vcc	VI	t _r /t _f	VM	VLOAD	CL	RL	\mathbf{v}_{Δ}
1.8 V \pm 0.15 V	Vcc	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	Vcc	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	VCC	≤2.5 ns	V _{CC} /2	2 × V _{CC}	50 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS PULSE DURATION





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ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

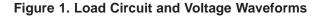
NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tPLZ and tPHZ are the same as tdis.

PROPAGATION DELAY TIMES

INVERTING AND NONINVERTING OUTPUTS

- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
CLVC1G374QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
CLVC1G374QDCKRQ1	ACTIVE	SC70	DCK	6	3000	Pb-Free (RoHS)	NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G374-Q1 :

• Catalog: SN74LVC1G374

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- È. Falls within JEDEC MO-178 Variation AB, except minimum lead width.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.



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